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Clean Version of Pending Claims

HIGH PERFORMANCE CAPACITOR
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1. A capacitor comprising:

a plurality of conductive layers embedded in a dielectric; and

a plurality of vias coupling at least two of the plurality of conductive layers to a plurality of connection sites.

N.E.

2. The capacitor of claim 1, wherein the capacitor has a thickness of between about .5 millimeter and about 1 millimeter.

3. The capacitor of claim 2, wherein the capacitor has a capacitance of between about 20 and about 30 microfarads.

SUB B/C1

4. (Amended) The capacitor of claim 1, wherein the plurality of connection sites have a pitch of between about 100 and about 500 microns.

N.E.

5. The capacitor of claim 1, wherein the plurality of vias are plated through holes.

SUB C1

B2

6. (Amended) A capacitor comprising:

a plurality of first conductive layers, each of the plurality of first conductive layers formed on a first dielectric sheet;

a plurality of second conductive layers, each of the plurality of second conductive layers formed on a second dielectric sheet, and the plurality of second conductive layers interlaced with the plurality of first conductive layers;

a pair of dielectric sheets, each of the pair of dielectric sheets having a thickness slightly greater than about 7 microns, for providing a pair of substantially rigid outer surfaces for the plurality of second conductive layers interlaced with the plurality of first conductive layers, each

of the pair of substantially rigid outer surfaces having a plurality of connection sites operable for coupling the capacitor to a substrate using a controlled collapse chip connection (C4); and

a plurality of vias coupling the plurality of first conductive layers and the plurality of second conductive layers to at least two of the plurality of connection sites.

7. The capacitor of claim 6, wherein each of the plurality of first conductive layers is fabricated from a tungsten paste.

8. The capacitor of claim 6, wherein the number of surfaces is two.

9. (Amended) A capacitor comprising:

a multilayered capacitor having a pair of substantially rigid outer surfaces; and

a plurality of pads located on the pair of substantially rigid outer surfaces wherein at least two of the plurality of pads are capable of being coupled to a substrate using a solder bump.

10. The capacitor of claim 9, wherein the multilayered capacitor includes a number of parallel conductive layers and the number of pads are coupled to the number of parallel conductive layers through vias.

11. The capacitor of claim 10, wherein the number of conductive layers is greater than about 50.

12. The capacitor of claim 11, wherein the number of pads is greater than about 4000.